Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A circuit for providing a switched high-voltage signal in response to an input logic-level state, comprising:

a first pFET having a source, drain, well and gate terminal, the source and well coupled to a source of a high-voltage signal, the drain coupled to an intermediate node and the gate coupled to a control node;

a second pFET having a source, drain, well and gate terminal, the source and well coupled to the intermediate node, the drain coupled to a voltage output node and providing the switched high-voltage signal, the gate coupled to a source of a first intermediate voltage, said first intermediate voltage being intermediate said high-voltage and a ground;

a diode having its anode coupled to a source of a second intermediate voltage, said second intermediate voltage being intermediate said high-voltage and the ground, and its cathode coupled to the intermediate node; and

a high-voltage MOS nFET having a source, drain and gate terminal, the source coupled to the ground, the drain coupled to the voltage output node and the gate coupled to a source of the input logic-level state.

2. (Original) The circuit of claim 1, wherein said first intermediate voltage and said second intermediate voltage are the same voltage.

3. (Original) The circuit of claim 1, wherein said high-voltage nFET includes a drain having an n+ region disposed in an n- well.

4. (Original) The circuit of claim 1, further comprising:

a pull-up circuit coupled to said control node, said high-voltage supply and a source of a bias signal.

5. (Original) The circuit of claim 2, further comprising:

a pull-up circuit coupled to said control node, said high-voltage supply and a source of a bias signal.

6. (Original) The circuit of claim 4 wherein said pull-up circuit comprises:

a pFET having a source and a well coupled to said high-voltage supply, a drain coupled to said control node, and a gate coupled to said source of said bias signal.

7. (Original) The circuit of claim 5, wherein said pull-up circuit comprises:

a pFET having a source and a well coupled to said high-voltage supply, a drain coupled to said control node, and a gate coupled to said source of said bias signal.

8. (Original) A circuit for providing a switched high-voltage signal in response to a first and a second logic level input, comprising:

a first pFET having a source, drain, well and gate terminal, the source and well coupled to a high-voltage supply, the drain coupled to an intermediate node and the gate coupled to a control node;

a second pFET having a source, drain, well and gate terminal, the source and well coupled to the intermediate node, the drain coupled to a voltage output node and providing the

switched high-voltage signal, the gate coupled to a source of a first intermediate voltage, said first intermediate voltage being intermediate said high-voltage supply and a ground;

a diode having its anode coupled to a source of a second intermediate voltage, said second intermediate voltage being intermediate said high-voltage and the ground, and its cathode coupled to the intermediate node;

a high-voltage MOS nFET having a source, drain and gate terminal, the source coupled to the ground, the drain coupled to the voltage output node and the gate coupled to a source of the first logic-level input;

a pull-up circuit coupled to said control node and to said high-voltage supply; and

a capacitor coupled at a first terminal to the second logic level input and at a second terminal to said control node and to said pull-up circuit.

9. (Original) The circuit of claim 8, wherein said first intermediate voltage and said second intermediate voltage are the same voltage.

10. (Original) The circuit of claim 8, wherein said high-voltage nFET includes a drain having an n+ region disposed in an n- well.

11. (Original) The circuit of claim 8, wherein said pull-up circuit comprises a pFET having a source and a well coupled to said high-voltage supply, a drain coupled to said second terminal of said capacitor, a gate coupled to said control node, and said gate and said drain coupled together.

12. (Original) The circuit of claim 9, wherein said pull-up circuit comprises a pFET having a source coupled to said high-voltage supply, a drain coupled to said second terminal of said capacitor, a gate coupled to said control node, and said gate and said drain coupled together.

13. (Original) A circuit for providing a switched high-voltage signal in response to an input logic-level state, comprising:

a first pFET having a source, drain, well and gate terminal, the source and well coupled to a source of a high-voltage signal, the drain coupled to a first intermediate node and the gate coupled to a control node;

a second pFET having a source, drain, well and gate terminal, the source and well coupled to the first intermediate node, the drain coupled to a voltage output node and providing the switched high-voltage signal, the gate coupled to a source of a first intermediate voltage, said first intermediate voltage being intermediate said high-voltage and a ground;

a first diode having its anode coupled to a source of a second intermediate voltage, said second intermediate voltage being intermediate said high-voltage and the ground, and its cathode coupled to the first intermediate node;

a MOS nFET having a source, drain and gate terminal, the source coupled to the ground, the drain coupled to a second intermediate node and the gate coupled to a source of the input logic-level state; and

a high-voltage MOS nFET having a source, drain and gate terminal, the source coupled to the drain of the MOS nFET, the drain coupled to the voltage output node and the gate coupled to a source of Vdd, said Vdd being a voltage between said intermediate voltages and the ground.

14. (Original) The circuit of claim 13, wherein said second intermediate node is coupled to the source of Vdd through a diode.

15. (Original) The circuit of claim 13, wherein said first intermediate voltage and said second intermediate voltage are the same voltage.

16. (Original) The circuit of claim 13, wherein said high-voltage nFET includes a drain having an n+ region disposed in an n- well.

17. (Original) The circuit of claim 13, further comprising:

a pull-up circuit coupled to said control node, said high-voltage supply and a source of a bias signal.

18. (Original) The circuit of claim 14, further comprising:

a pull-up circuit coupled to said control node, said high-voltage supply and a source of a bias signal.

19. (Original) The circuit of claim 15, further comprising:

a pull-up circuit coupled to said control node, said high-voltage supply and a source of a bias signal.

20. (Original) The circuit of claim 18 wherein said pull-up circuit comprises:

a pFET having a source and a well coupled to said high-voltage supply, a drain coupled to said control node, and a gate coupled to said source of said bias signal.

21. (Original) The circuit of claim 19 wherein said pull-up circuit comprises:

a pFET having a source and a well coupled to said high-voltage supply, a drain coupled to said control node, and a gate coupled to said source of said bias signal.

22. (Original) A circuit for providing a switched high-voltage signal in response to a first and a second logic level input, comprising:

a first pFET having a source, drain, well and gate terminal, the source and well coupled to a high-voltage supply, the drain coupled to a first intermediate node and the gate coupled to a control node;

a second pFET having a source, drain, well and gate terminal, the source and well coupled to the first intermediate node, the drain coupled to a voltage output node and providing the switched high-voltage signal, the gate coupled to a source of a first intermediate voltage, said first intermediate voltage being intermediate said high-voltage supply and a ground;

a first diode having its anode coupled to a source of a second intermediate voltage, said second intermediate voltage being intermediate said high-voltage and the ground, and its cathode coupled to the first intermediate node;

a MOS nFET having a source, drain and gate terminal, the source coupled to the ground, the drain coupled to a second intermediate node and the gate coupled to a source of the input logic-level state; and

a high-voltage MOS nFET having a source, drain and gate terminal, the source coupled to the drain of the MOS nFET, the drain coupled to the voltage output node and the gate coupled to a source of Vdd, said Vdd being a voltage between said first and second intermediate voltages and the ground; and

a pull-up circuit coupled to said control node and to said high-voltage supply.

23. (Original) The circuit of claim 22, further comprising:

capacitor coupled at a first terminal to the second logic-level input and at a second terminal to said control node and to said pull-up circuit.

24. (Original) The circuit of claim 22, wherein said first intermediate voltage and said second intermediate voltage are the same voltage.

25. (Original) The circuit of claim 23, wherein said first intermediate voltage and said second intermediate voltage are essentially the same voltage.

26. (Original) The circuit of claim 22, wherein said high-voltage nFET includes a drain having an n+ region disposed in an n- well.

27. (Original) The circuit of claim 23, wherein said high-voltage nFET includes a drain having an n+ region disposed in an n- well.

28. (Original) The circuit of claim 22, wherein said pull-up circuit comprises:

a pFET having a source and a well coupled to said high-voltage supply, a drain coupled to said second terminal of said capacitor, a gate coupled to said control node, and said gate and said drain coupled together.

29. (Original) The circuit of claim 23, wherein said pull-up circuit comprises:

a pFET having a source and a well coupled to said high-voltage supply, a drain coupled to said second terminal of said capacitor, a gate coupled to said control node, and said gate and said drain coupled together.

30. (Original) The circuit of claim 24, wherein said pull-up circuit comprises a pFET having a source coupled to said high-voltage supply, a drain coupled to said second terminal of said capacitor, a gate coupled to said control node, and said gate and said drain coupled together.

31. (Original) A circuit for providing a switched high-voltage signal in response to an input logic-level state, comprising:

a first pFET having a drain capacitively coupled to a first logic input node, a source coupled to a first high-voltage supply node and a gate electrically coupled to said drain of said first pFET and to a control node;

a second pFET having a source coupled to a second high-voltage supply node, a gate coupled to said control node and a drain coupled to a first node;

a third pFET having a source coupled to said first node, a gate coupled to an intermediate voltage source node and a drain coupled to an output voltage node;

a diode coupled to conduct from a second intermediate voltage-source node to said first node; and

a high-voltage nFET having a drain coupled to said output voltage node, a gate coupled to a second logic input node and a source coupled to a ground.

32. (Original) The circuit of claim 31, wherein said first logic input node and said second logic input node are electrically coupled.

33. (Original) The circuit of claim 31, wherein said first high-voltage supply node and said second high-voltage supply node are electrically coupled.

34. (Original) The circuit of claim 31, wherein said first intermediate voltage-source node and said second intermediate voltage-source node are electrically coupled.

35. (Original) The circuit of claim 31, wherein said high-voltage nFET includes a drain having an n+ region disposed in an n- well.

36. (Original) A circuit for providing a switched high-voltage signal in response to an input logic-level state, comprising:

a first pFET having a gate coupled to a bias signal node, a source coupled to a first high-voltage supply node and a drain coupled to a control node;

a second pFET having a source coupled to a second high-voltage supply node, a gate coupled to said control node and a drain coupled to a first node;

a third pFET having a source coupled to said first node, a gate coupled to an intermediate voltage-source node and a drain coupled to an output voltage node;

a diode coupled to conduct from a second intermediate voltage source node to said first node; and

a high-voltage nFET having a drain coupled to said output voltage node, a gate coupled to a logic input node and a source coupled to a ground.

37. (Original) The circuit of claim 36, wherein said first high-voltage supply node and said second high-voltage supply node are electrically coupled.

38. (Original) The circuit of claim 36, wherein said bias signal node is coupled to a bias voltage adjusted to cause said first pFET to source a current.

39. (Original) The circuit of claim 36, wherein said first intermediate voltage-source node and said second intermediate voltage-source node are electrically coupled.

40. (Original) The circuit of claim 36, wherein said high-voltage nFET includes a drain having an n+ region disposed in an n- well.

41. (Original) A circuit for providing a switched high-voltage signal in response to an input logic-level state, comprising:

a set-reset latch circuit having a set node for receiving a set logic level input, a reset node for receiving a reset logic level input, and a control node;

a first pFET having a source coupled to a first high-voltage supply node, a gate coupled to said control node and a drain coupled to a first node;

a second pFET having a source coupled to said first node, a gate coupled to a first intermediate voltage source node and a drain coupled to an output voltage node;

a first diode coupled to conduct from a second intermediate voltage source node to said first node; and

a first high-voltage nFET having a drain coupled to said output voltage node, a gate coupled to a logic input node and a source coupled to a ground.

42. (Original) The circuit of claim 41, wherein said first intermediate voltage-source node and said second intermediate voltage-source node are electrically coupled.

43. (Original) The circuit of claim 41, wherein said first high-voltage nFET includes a drain having an n+ region disposed in an n- well.

44. (Original) The circuit of claim 41, wherein said set-reset latch circuit comprises:

a second high-voltage nFET having a gate coupled to said reset node, a source coupled to a ground, and a drain coupled to a second node;

a third high-voltage nFET having a gate coupled to said set node, a source coupled to the ground and a drain coupled to a third node;

a second diode coupled to conduct from a third intermediate voltage source node to said second node, said third intermediate voltage being between said first high-voltage and the ground;

a third diode coupled to conduct from a fourth intermediate voltage source node to said third node, said fourth intermediate voltage being between said first high-voltage and the ground;

a third pFET having a source coupled to a second high-voltage supply node, a gate coupled to said third node, and a drain coupled to said second node; and

a fourth pFET having a source coupled to a third high-voltage supply node, a gate coupled to said second node, and a drain coupled to said third node and to said control node.

45. (Original) The circuit of claim 44, wherein said second high-voltage supply node and said third high-voltage supply node are electrically coupled.

46. (Original) The circuit of claim 44, wherein said first intermediate voltage-source node and said second intermediate voltage-source node are electrically coupled.

47. (Original) The circuit of claim 44, wherein said third intermediate voltage-source node and said fourth intermediate voltage-source node are electrically coupled.

48. (Original) The circuit of claim 46, wherein said first intermediate voltage-source node and said third intermediate voltage-source node are electrically coupled.

49. (Original) The circuit of claim 48, wherein said first intermediate voltage-source node and said fourth intermediate voltage-source node are electrically coupled.

50. (Original) The circuit of claim 45, wherein said first high-voltage supply node and said second high-voltage supply node are electrically coupled.

51. (Original) The circuit of claim 44, wherein said first high-voltage nFET includes a drain having an n+ region disposed in an n- well.

52. (Original) The circuit of claim 51, wherein said second high-voltage nFET includes a drain having an n+ region disposed in an n- well.

53. (Original) The circuit of claim 52, wherein said third high-voltage nFET includes a drain having an n+ region disposed in an n- well.

54. (Original) A circuit for providing a switched high-voltage signal in response to an input logic-level state, comprising:

a first pFET having a gate coupled to a bias signal node, a source coupled to a first high-voltage supply node and a drain coupled to a control node;

a second pFET having a source coupled to a second high-voltage supply node, a gate coupled to said control node and a drain coupled to a first node;

a third pFET having a source coupled to said first node, a gate coupled to a first intermediate voltage source node and a drain coupled to an output voltage node;

a first diode coupled to conduct from a second intermediate voltage source node to said first node; and

a first high-voltage nFET having a drain coupled to said output voltage node, a gate coupled to a first logic input node and a source coupled to a ground.

55. (Original) The circuit of claim 54, wherein said first intermediate voltage source node and said second intermediate voltage source node are electrically coupled.

56. (Original) The circuit of claim 54, wherein said first high-voltage supply node and said second high-voltage supply node are electrically coupled.

57. (Original) The circuit of claim 54, wherein said bias signal node is coupled to a bias voltage adjusted to cause said first pFET to source a current.

58. (Original) The circuit of claim 54, further comprising:

a third intermediate-voltage source node coupled through a second diode to said control node.

59. (Original) The circuit of claim 54, wherein said first high-voltage nFET includes a drain having an n+ region disposed in an n- well.

60. (Original) The circuit of claim 59, further comprising:

a second high-voltage nFET having a drain coupled to said control node, a gate coupled to a second logic input node and a source coupled to a ground.

61. (Original) The circuit of claim 59, wherein said second high-voltage nFET includes a drain having an n+ region disposed in an n- well.

62. (Original) A circuit for providing a switched high-voltage signal in response to an input logic level state, comprising:

a first pFET having a source coupled to a source of high-voltage, a drain coupled to an intermediate node and a gate coupled to a control node;

a second pFET having a source coupled to said intermediate node, a drain coupled to an output node and a gate coupled to a first intermediate voltage source, said first intermediate voltage source providing a voltage between said high-voltage and a ground;

a second intermediate voltage source coupled through a diode to said intermediate node, said second intermediate voltage source also providing a voltage between said high-voltage and ground; and

a high-voltage nFET having a drain coupled to said output node, a source coupled to ground and a gate coupled to a logic input node.

63. (Original) The circuit of claim 62, wherein said first intermediate voltage source and said second intermediate voltage source provide essentially the same voltage.

64. (Original) The circuit of claim 62, wherein said diode has its anode coupled to said gate of said second pFET and its cathode coupled to said intermediate node.

65. (Original) The circuit of claim 64, wherein said diode is formed from a diode-connected pFET.

66. (Original) The circuit of claim 64, wherein said diode is formed from a diode-connected nFET.

67. (Original) The circuit of claim 66, wherein said high-voltage nFET includes a drain having an n+ region disposed in an n- well.

68. (Original) A circuit for providing a switched high-voltage signal in response to an input logic-level state, comprising:

a first high-voltage nFET having a gate coupled to Vdd, a source coupled to a first logic-level input node, and a drain coupled to a control node;

a first pFET having a source coupled to a source of high-voltage, a drain coupled to an intermediate node and a gate coupled to a control node;

a second pFET having a source coupled to said intermediate node, a drain coupled to an output node and a gate coupled to a first source of an intermediate voltage intermediate said high voltage and ground;

a second source of an intermediate voltage intermediate said high-voltage and ground coupled through a diode to said intermediate node; and

a second high-voltage nFET having a drain coupled to said output node, a source coupled to ground and a gate coupled to a second logic-level input node.

69. (Original) The circuit of claim 68, wherein said diode has its anode coupled to said gate of said second pFET and its cathode coupled to said intermediate node.

70. (Original) The circuit of claim 69, wherein said diode is formed from a diode-connected pFET.

71. (Original) The circuit of claim 68, wherein said first and said second high-voltage nFETs include drains having n+ regions disposed in n- wells.

72. (Original) The circuit of claim 68, wherein said first source of an intermediate voltage and said second source of an intermediate voltage are electrically coupled.

73. (Original) The circuit of claim 68, wherein said first source of an intermediate voltage and said second source of an intermediate voltage provide essentially the same voltage.

74. (Original) A circuit for providing a switched high-voltage signal in response to an input logic-level state, comprising:

a first and a second high-voltage nFET each having a gate coupled to Vdd, each having a source coupled to a logic-level input node, one of said logic-level input nodes being an inverse of

the other, and each having a drain coupled to an output node, one of said output nodes being an inverse of the other;

a first and a second pFET having their sources coupled to a source of high-voltage, and their gates and drains cross-coupled; and

an intermediate voltage stage including a third and a fourth pFET, sources of the respective third and fourth pFETs coupled to drains of the respective first and second pFETs, sources of the respective third and fourth pFETs coupled through respective first and second diodes to respective first and second intermediate voltage nodes, gates of said respective third and fourth pFETs coupled respectively to said first and second intermediate voltage nodes, and drains of said respective third and fourth pFETs coupled respectively to drains of said first and second high-voltage nFETs.

75. (Original) The circuit of claim 74, wherein said first and said second high-voltage nFETs include drains having n+ regions disposed in n- wells.

76. (Original) The circuit of claim 74, wherein said first and second intermediate voltages are substantially the same voltage.

77. (Original) A circuit for providing a differential switched high-voltage signal in response to a pair of complementary Reset-Set input logic-level signals, comprising:

a first and a second pFET each having a source, drain, well and gate terminal, the source and well of each coupled to a high-voltage supply, the drain of the second pFET coupled to a first intermediate node and its gate coupled to a second intermediate node, the drain of the first pFET coupled to the second intermediate node and its gate coupled to the first intermediate node;

a first circuit portion responsive to the Set signal and a Preset signal coupled to the first intermediate node to enable assertion of the Set signal to the first intermediate node when the Preset signal is asserted;

a second circuit portion responsive to the Reset signal and the Preset signal coupled to the second intermediate node to enable assertion of the Reset signal to the second intermediate node when the Preset signal is asserted;

a third and fourth pFET, said third pFET having its source coupled to the first intermediate node, its drain coupled to a first of two complementary switched voltage output nodes and its gate coupled to an intermediate-voltage supply, and said fourth pFET having its source coupled to the second intermediate node, its drain coupled to the second of two complementary switched voltage output nodes and its gate coupled to the intermediate-voltage supply; and

a first and a second high-voltage circuit portion, said first high-voltage circuit portion coupling the first of two complementary switched voltage output nodes to a ground through a circuit element responsive to the Reset signal, said second high-voltage circuit portion coupling the second of two complementary switched voltage output nodes to the ground through a circuit element responsive to the Set signal.

78. (Original) The circuit of claim 77, further comprising a first diode coupled between said first intermediate node and a ground.

79. (Original) The circuit of claim 78, further comprising a second diode coupled between said second intermediate node and a ground.

80. (Original) The circuit of claim 79, wherein said first and second diodes are n-well diodes having their respective anodes coupled to the ground and their respective cathodes coupled to said first intermediate node and said second intermediate node, respectively.

81. (Original) The circuit of claim 77, further comprising:

a first and a second n- well diode, said first n- well diode having an anode coupled to a ground and a cathode coupled to the first intermediate node, said second n- well diode having an anode coupled to the ground and a cathode coupled to the second intermediate node.

82. (Original) The circuit of claim 77, wherein said first and second high-voltage circuit portion comprise:

a first and a second high-voltage nFET, said first high-voltage nFET having its drain coupled to the first of two complementary switched voltage output nodes, its gate coupled to a Vdd supply, and its source coupled to the ground through a first transistor responsive to the Reset signal, said second high-voltage nFET having its drain coupled to the second of two complementary switched voltage output nodes, its gate coupled to the Vdd supply, and its source coupled to ground through a second transistor responsive to the Set signal.

83. (Original) The circuit of claim 77, wherein said first circuit portion comprises a high-voltage nFET having its drain coupled to the first intermediate node, its gate coupled to the Vdd supply and its source coupled to the source of the Set signal through a transistor responsive to the Preset signal.

84. (Original) The circuit of claim 83, wherein said second circuit portion comprises a high-voltage nFET having its drain coupled to the second intermediate node, its gate coupled to the Vdd supply and its source coupled to the source of the Reset signal through a transistor responsive to the Preset signal.

85. (Original) The circuit of claim 84, wherein the transistor responsive to the Set signal is an nFET and the source of the Preset signal is coupled to its gate and the source of the Set signal is coupled to its source.

86. (Original) The circuit of claim 85, wherein the transistor responsive to the Reset signal is an nFET and the source of the Preset signal is coupled to its gate and the source of the Reset signal is coupled to its source.

87. (Original) The circuit of claim 79, wherein said first transistor is an nFET having its drain coupled to the source of the first high-voltage nFET, its gate coupled to a source of the Reset signal and its drain coupled to the ground.

88. (Original) The circuit of claim 87, wherein said second transistor is an nFET having its drain coupled to the source of the second high-voltage nFET, its gate coupled to a source of the Set signal and its drain coupled to the ground.

89. (Original) The circuit of claim 77, wherein the intermediate-voltage is set to a level between Vdd and the high-voltage supply.

90. (Currently amended) A circuit for providing a differential switched high-voltage signal in response to a pair of complementary Reset-Set input logic-level signals, comprising:

a first and a second pFET each having a source, drain, well and gate terminal, the source and well of each coupled to a high-voltage supply, the drain of the first pFET coupled to a first intermediate node and its gate coupled to a second intermediate node, the drain of the second pFET coupled to the second intermediate node and its gate coupled to the first intermediate node;

a third and fourth pFET, said third pFET having its source coupled to the first intermediate node, its drain coupled to a first of two complementary switched voltage output nodes and its gate coupled to an intermediate-voltage supply, and said fourth pFET having its source coupled to the second intermediate node, its drain coupled to the second of two complementary switched voltage output nodes and its gate coupled to the intermediate-voltage supply; ~~and~~

a first and a second high-voltage circuit portion, said first high-voltage circuit portion coupling the first of the two complementary switched voltage output nodes to a ground through a circuit element responsive to the Reset signal, said second high-voltage circuit portion coupling the second of two complementary switched voltage output nodes to the ground through a circuit element responsive to the Set signal[[.]];

a first diode having an anode coupled to said intermediate-voltage supply and a cathode coupled to said first intermediate node; and

a second diode having an anode coupled to said intermediate-voltage supply and a cathode coupled to said second intermediate node.

91. (Original) The circuit of claim 90, wherein said first and second high-voltage circuit portion comprise:

a first and a second high-voltage nFET, said first high-voltage nFET having its drain coupled to the first of two complementary switched voltage output nodes, its gate coupled to a Vdd supply, and its source coupled to the ground through a first transistor responsive to the Reset signal, said second high-voltage nFET having its drain coupled to the second of two complementary switched voltage output nodes, its gate coupled to the Vdd supply, and its source coupled to ground through a second transistor responsive to the Set signal.

92. (Canceled)

93. (Currently amended) The circuit of claim ~~92~~ 90, further comprising:

a fifth pFET and sixth pFET, said fifth pFET having its source and well coupled to the drain of said third pFET, its gate coupled to said intermediate-voltage supply and its drain coupled to the first of two complementary switched voltage output nodes, said sixth pFET having its source and well coupled to the drain of said fourth pFET, its gate coupled to said intermediate-voltage supply and its drain coupled to the second of two complementary switched voltage output nodes.

94. (Original) The circuit of claim 93, further comprising:

a third diode having an anode coupled to said intermediate-voltage supply and a cathode coupled to said source of said fifth pFET; and

a fourth diode having an anode coupled to said intermediate-voltage supply and a cathode coupled to said source of said sixth pFET.

95. (Original) The circuit of claim 94, wherein said first and second high-voltage circuit portion comprise:

a first and a second high-voltage nFET, said first high-voltage nFET having its drain coupled to the first of two complementary switched voltage output nodes, its gate coupled to a Vdd supply, and its source coupled to the ground through a first transistor responsive to the Reset signal, said second high-voltage nFET having its drain coupled to the second of two complementary switched voltage output nodes, its gate coupled to the Vdd supply, and its source coupled to ground through a second transistor responsive to the Set signal.

96. (Original) A circuit for providing a differential switched high-voltage signal in response to a pair of complementary Reset-Set input logic-level signals, comprising:

a first and a second pFET each having a source, drain, well and gate terminal, the source and well of each coupled to a high-voltage supply, the drain of the first pFET coupled to a first intermediate node and its gate coupled to a second intermediate node, the drain of the second pFET coupled to the second intermediate node and its gate coupled to the first intermediate node;

a first and a second n- well diode, said first n- well diode having an anode coupled to a ground and a cathode coupled to the first intermediate node, said second n- well diode having an anode coupled to the ground and a cathode coupled to the second intermediate node;

a third and fourth pFET, said third pFET having its source coupled to the first intermediate node, its well coupled to the high-voltage supply, its drain coupled to a first of two complementary switched voltage output nodes and its gate coupled to an intermediate-voltage supply, and said fourth pFET having its source coupled to the second intermediate node, its well coupled to the high-voltage supply, its drain coupled to the second of two complementary switched voltage output nodes and its gate coupled to the intermediate-voltage supply; and

a first and a second high-voltage circuit portion, said first high-voltage circuit portion coupling the first of two complementary switched voltage output nodes to a ground through a circuit element responsive to the Reset signal, said second high-voltage circuit portion coupling the second of two complementary switched voltage output nodes to the ground through a circuit element responsive to the Set signal.

97. (Original) The circuit of claim 96, wherein said first and second high-voltage circuit portion comprise:

a first and a second high-voltage nFET, said first high-voltage nFET having its drain coupled to the first of two complementary switched voltage output nodes, its gate coupled to a Vdd supply, and its source coupled to the ground through a first transistor responsive to the Reset signal, said second high-voltage nFET having its drain coupled to the second of two complementary switched voltage output nodes, its gate coupled to the Vdd supply, and its source coupled to ground through a second transistor responsive to the Set signal.

98. (Original) The circuit of claim 96, further comprising:

a first diode having an anode coupled to said intermediate-voltage supply and a cathode coupled to said drain of aid third pFET; and

a second diode having an anode coupled to said intermediate-voltage supply and a cathode coupled to said drain of said fourth pFET.

99. (Original) The circuit of claim 98, further comprising:

a fifth pFET and sixth pFET, said fifth pFET having its source and well coupled to the drain of said third pFET, its gate coupled to said intermediate-voltage supply and its drain

coupled to the first of two complementary switched voltage output nodes, said sixth pFET having its source and well coupled to the drain of said fourth pFET, its gate coupled to said intermediate-voltage supply and its drain coupled to the second of two complementary switched voltage output nodes.

100. (Original) The circuit of claim 99, wherein said first and second high-voltage circuit portion comprise:

a first and a second high-voltage nFET, said first high-voltage nFET having its drain coupled to the first of two complementary switched voltage output nodes, its gate coupled to a Vdd supply, and its source coupled to the ground through a first transistor responsive to the Reset signal, said second high-voltage nFET having its drain coupled to the second of two complementary switched voltage output nodes, its gate coupled to the Vdd supply, and its source coupled to ground through a second transistor responsive to the Set signal.